CLAIMS

1. A non-volatile passive matrix memory device (10) comprising an electrically polarizable dielectric memory material (12) exhibiting hysteresis, particularly a ferroelectric material, wherein said memory material (12) is provided sandwiched in a layer between a first set and second set (14;15) of respective parallel addressing electrodes, wherein the electrodes of the first set (14) constitute word lines ($WL_{1,...m}$) of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set (15), the latter constituting bit lines ($BL_{1,...n}$) of the memory device, wherein a memory cell (13) with a capacitor-like structure is defined in the memory material (12) at the crossings between word lines and bit lines, wherein the memory cells (13) of the memory device constitute the elements of a passive matrix (11), wherein each memory cell (13) can be selectively addressed for a write/read operation via a word line (WL) and bit line (BL), wherein a write operation to a memory cell (13) takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line (WL) and bit line (BL) defining the cell, wherein said applied voltage either establishes a determined polarization state in the memory cell (13) or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage smaller than the switching or polarization voltage V_s to the memory cell (13) and detecting at least one electrical parameter of an output current on the bit lines (BL),
characterized in that
the word lines (WL) are divided into a number of segments ($S_{1,...q}$), each segment comprising and being defined by a plurality of adjoining bit lines (BL) in the matrix (11), and that means (25) are provided for connecting each bit line (BL) assigned to a segment (S) with an associated sensing means (26), thus enabling simultaneous connection of all memory cells (13) assigned to a word line (WL) on a segment (S) for readout via the corresponding bit lines (BL) of the segment (S), each sensing means (26) being adapted for sensing the charge flow in the bit line (BL) connected therewith in order to determine a logical value stored in the memory cell (13) defined by the bit line.

2. A non-volatile passive matrix memory device (10) according to claim 1, characterized in that said means (25) for simultaneous connection of each bit line

(BL) of a segment (S) with associated sensing means (26) during addressing are multiplexers.

3. A non-volatile passive matrix memory device (10) according to claim 2, characterized in that the number of multiplexers (25) corresponds to the largest number of bit lines (BL) defining a segment (S), each bit line of a segment being connected with a specific multiplexer.

4. A non-volatile passive matrix memory device (10) according to claim 3, characterized in that the output of each multiplexer (25) is connected with a single sensing means (26).

5. A non-volatile passive matrix memory device according to claim 4, characterized in that the single sensing means (26) is a sense amplifier.

6. A non-volatile passive matrix memory device according to claim 1, characterized in that said means (25) for simultaneous connection of each bit line (BL) of a segment (S) to an associated sensing means (26) during addressing is a gate means.

7. A non-volatile passive matrix memory device according to claim 6, characterized in that all bit lines ($BL_{1,...n}$) of a segment (S) are connected with a specific gate means, each gate means having a number of outputs corresponding to the number of bit lines (BL) in the respective segment (S), that each output of each gate means (25) is connected with a specific bus line (27) of an output data bus (28), the number of bus lines (27) thus corresponding to largest number of bit lines (BL) in a segment (S), and that each bus line (27) is connected with a single sensing means (26).

8. A non-volatile passive matrix memory device according to claim 6, characterized in that the gate means (25) comprise pass gates.

9. A non-volatile passive matrix memory device according to claim 6, characterized in that the sensing means (26) is a sense amplifier.

10. A method for readout of a non-volatile passive matrix memory device (10) comprising an electrically polarizable dielectric memory material (12) exhibiting hysteresis, particularly a ferroelectric material, wherein said memory material (12) is provided sandwiched in a layer between a first set and second set (14;15) of respective parallel addressing electrodes, wherein the electrodes of the first set (14) constitute word lines (WL) of the memory

device (10) and are provided in substantially orthogonal relationship to the electrodes of the second set (15), the latter constituting bit lines ($BL_{1,...n}$) of the memory device (10), wherein a memory cell (13) with a capacitor-like structure is defined in the memory material (12) at crossings between word lines (WL) and bit lines (BL), wherein the memory cells (13) of the memory device (10) constitute the elements of a passive matrix (11), wherein each memory cell (13) can be selectively addressed for a write/read operation via a word line (WL) and bit line (BL), wherein write operation to a memory cell (13) takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line (WL) and bit line (BL) defining the cell, said applied voltage either establishing a determined polarization state in the cell or being able to switch the cell between the polarization states thereof, wherein a read operation takes place by applying a voltage smaller than the switching or polarization voltage V_s to the memory cell (13) and detecting at least one electrical parameter of an output current on its bit lines (BL), and wherein the method comprises steps for controlling electric potentials on all word lines (WL) and bit lines (BL) in a time-coordinated fashion according to a protocol comprising electric timing sequences for all word lines and bit lines,
arranging said protocol to comprise a read cycle, and
providing during the read cycle for the sensing means to sense charges flowing in the bit lines, and wherein the method is characterized by
dividing the word lines (WL) into a number of segments ($S_1,...S_q$), each segment comprising and being defined by a number of adjacent bit lines (BL) in the matrix (11), connecting each bit line (BL) within a word line segment (S) with an associated sensing means (26),
activating according to the protocol one word line (WL) of a segment (S) at a time by setting the potential of said one word line (WL) of the segment (S) to the switching voltage V_s during at least a portion of the read cycle, while keeping all bit lines of the segment (S) at zero potential, and
determining the logical value stored in the individual memory cells (13) sensed by the sensing means (26) during the read cycle.

11. Method for readout according to claim 10,
characterized by
keeping all word lines (WL) and bit lines (BL) when no memory cell (13) is read or written, at a quiescent voltage of approximately □ of the switching voltage V_s,

activating according to the protocol one word line (WL) at a time by setting the potential of said one word line (WL) of the segment (S) to the switching voltage V_s during at least a portion of the read cycle, while keeping all bit lines (BL) of the segment (S) at zero potential, and

determining the logical value stored in the individual memory cells (13) sensed by the sensing means (26) during the read cycle.

12. The use of a non-volatile passive matrix memory device (10) according to claim 1 and a method for readout according to claim 10 in a volumetric data storage apparatus with a plurality of stacked layers (P_1, P_2,...), each layer (P) comprising one of the non-volatile passive matrix memory devices (10).